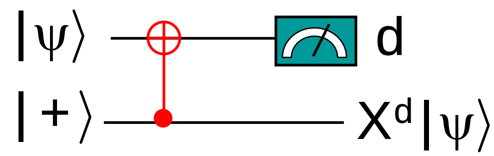
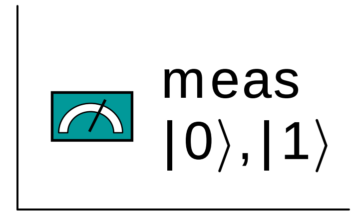
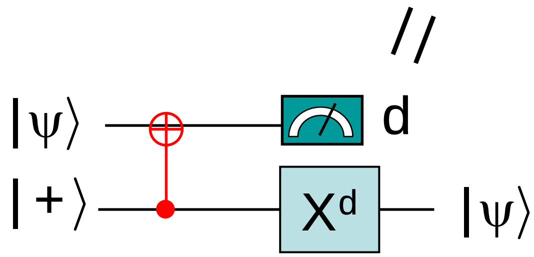
# Encoded non Clifford gate on the 7-bit code:

It is easy to verify this
"1-bit teleportation circuit"




If $\theta = \pi/8$,

$U X U^\dagger = U (XU^\dagger X) X$

$= e^{iZ\pi/8} (X e^{-iZ\pi/8} X) X$

$= e^{iZ\pi/8} e^{-iXZX\pi/8} X$

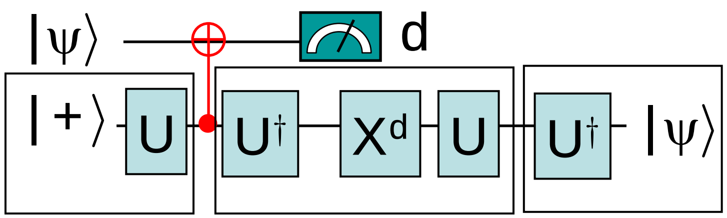
$= e^{iZ\pi/8} e^{+iZ\pi/8} X$

$= e^{iZ\pi/4} X \in C_2$

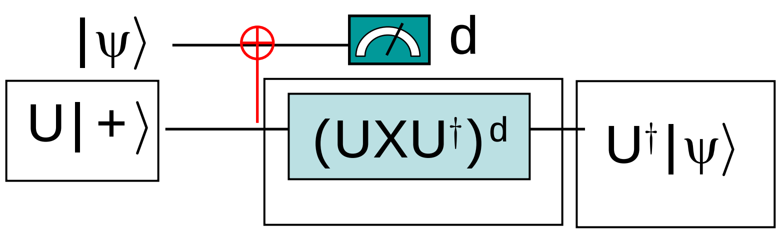
In fact, $U \in C_3$

Let $U = e^{i\theta Z}$

Then:




Then:



## Encoded non Clifford gate on the 7-bit code:

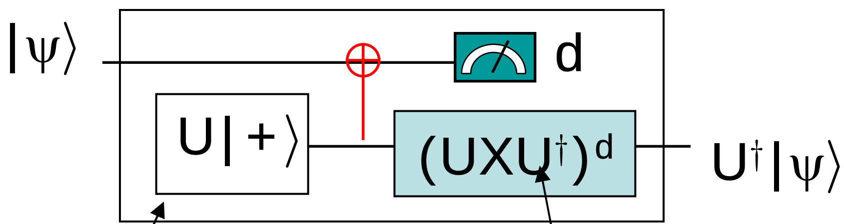
If $\theta = \pi/8$, $U = e^{iZ\pi/8}$ , then $U X U^\dagger = e^{iZ\pi/4} X \in C_2$

Circuit still holds if everything is in the encoded form !

bitwise cnot

encoded input

measure $Z_L$ (wait until FT)




Circuit performs encoded $U^\dagger$

state with stabilizer $UXU^\dagger$ (property (5)) will measure this stabilizer (wait until FT)

Clifford -- we know how to

## Standard (circuit) model of QC:

(1) Prepare $|0\rangle^{\otimes n}$

(2) execute universal set of gates

(3) measure in $|0\rangle$, $|1\rangle$ basis

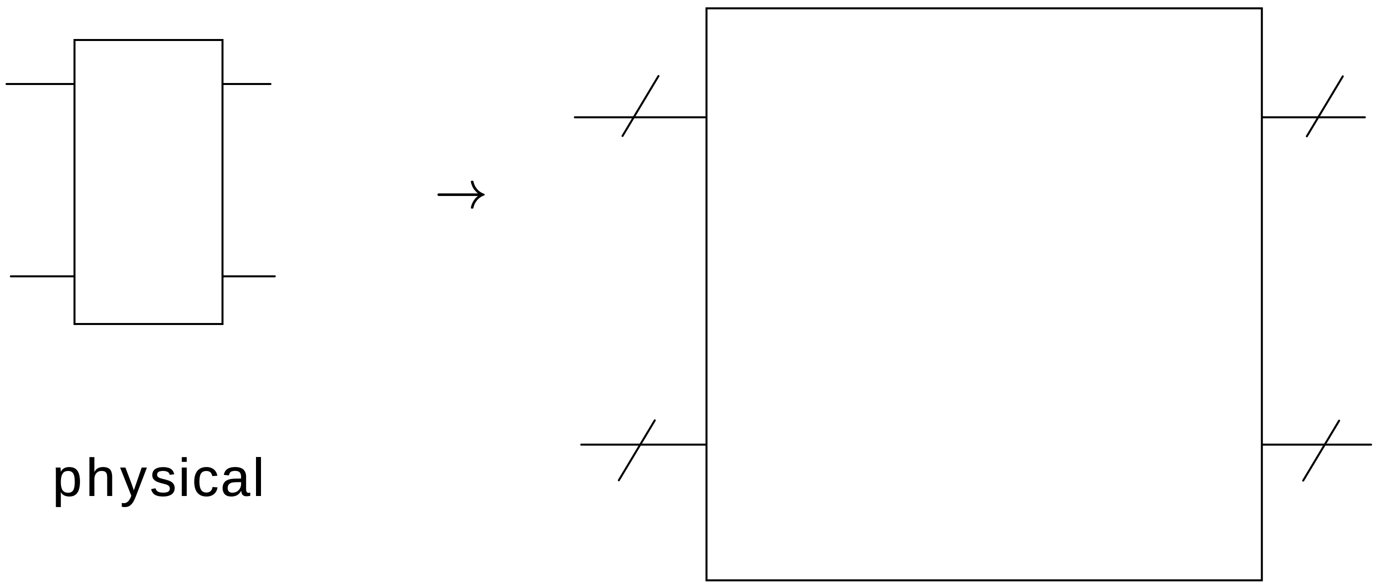
## Fault tolerant quantum computation

Goal: simulate any quantum circuit and obtain the ideal final measurement outcome (statistics) using imperfect operations.
If storage and operation noise are're too high, QECC may still work

Issues: gates for QECC are themselves noisy, measurements can be incorrect, errors can propagate via operations or syndrome measurements

Techniques:
Use QECC from the beginning (prepare $|0_L\rangle$)
Operate on encoded data, never decode and expose it to noise
Encoded gatess and measurement should not propagate errors
Perform EC often, and syndrome measurement should be repeated for correctness.

Hope 1: Error reduction by FT ops

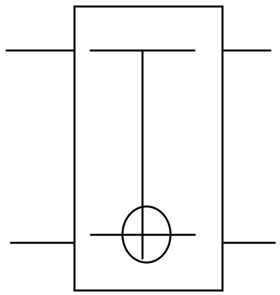


physical

encoded

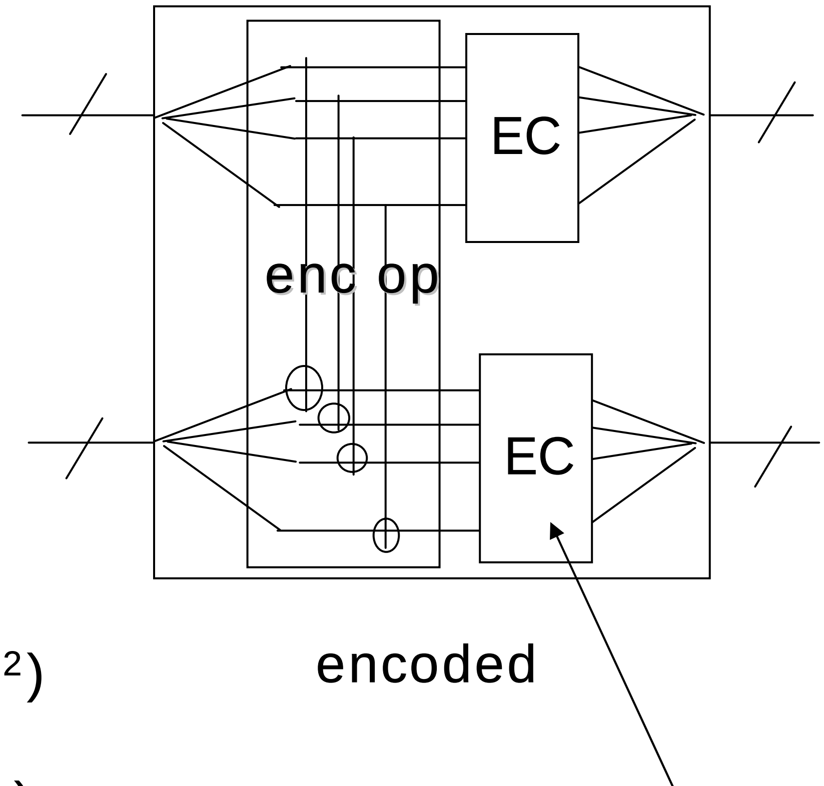
## Hope 1: Error reduction by FT ops

e.g.



physical

$\rightarrow$

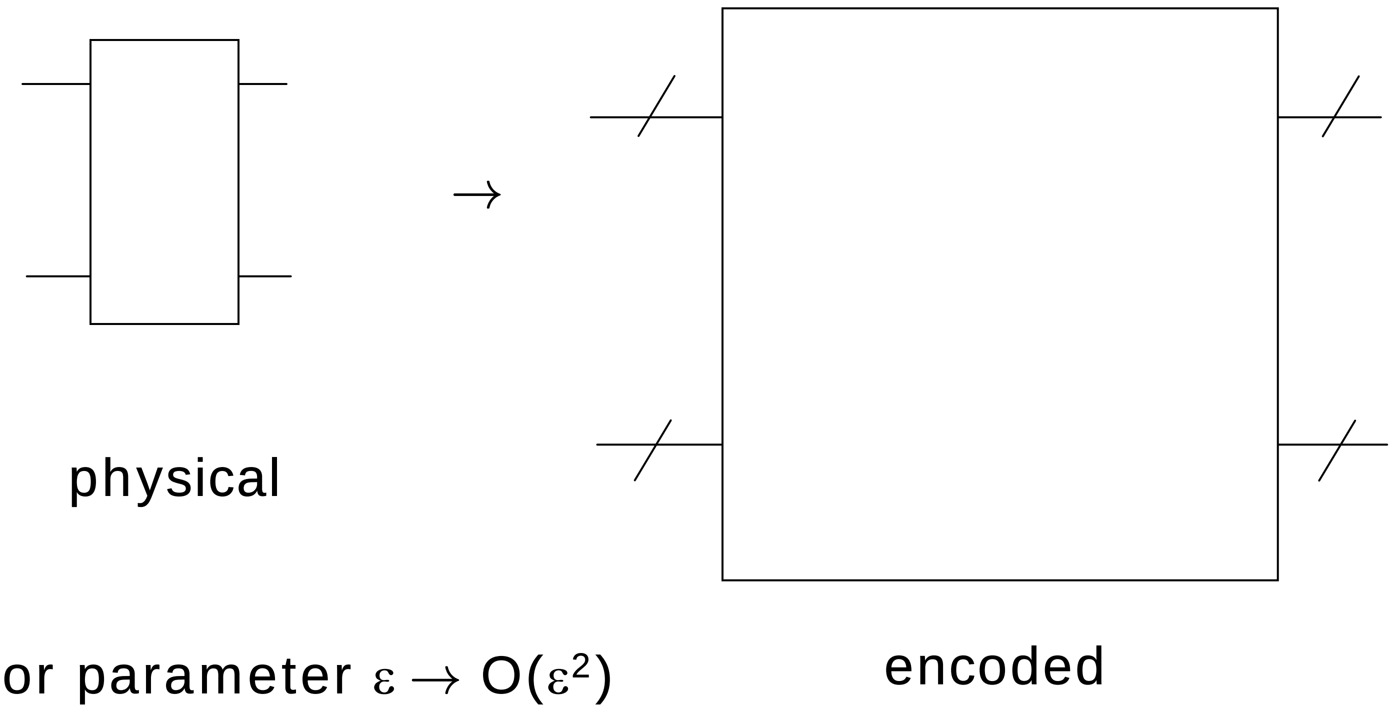



encoded

syndrome meas
+ reversion of error

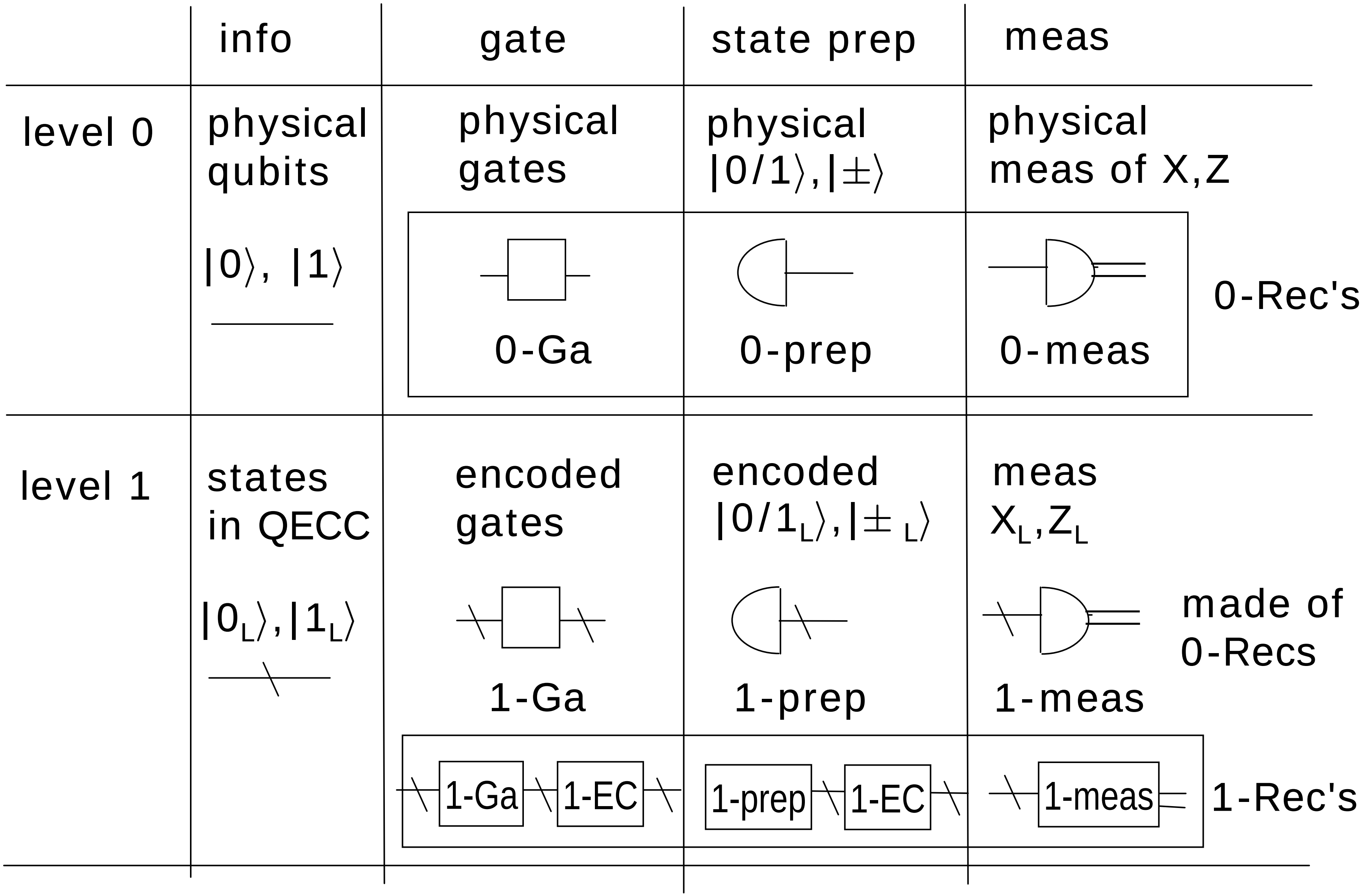
Want:
(1) error parameter $\varepsilon \rightarrow O(\varepsilon^2)$
[to actually reduce error]
(2) physical noise (TCP map) $\rightarrow$ similar TCP map on the encoded space, except for the parameter
[to enable recursive reduction]

Hope 1: Error reduction by FT ops




Want:
(1) error parameter $\varepsilon \rightarrow O(\varepsilon^2)$
[to actually reduce error]
(2) physical noise (TCP map) $\rightarrow$ similar TCP map on the encoded space, except for the parameter
[to enable recursive reduction]

Need (a) definition of FT ops s.t. (1), (2) holds
(b) actual FT ops for all circuit components


info
gate
state prep
meas
level 0
physical qubits
physical gates
physical |0/1⟩,|±⟩
physical meas of X,Z
|0⟩, |1⟩
0-Ga
0-prep
0-meas
0-Rec's
level 1
states in QECC
encoded gates
encoded |0/1_L⟩,|± _L⟩
meas X_L,Z_L
|0_L⟩,|1_L⟩
1-Ga
1-prep
1-meas
made of 0-Recs
1-Ga
1-EC
1-prep
1-EC
1-meas
1-Rec's

A 1-Rec is made of 0-Recs.

A 2-Rec is formed from a 1-Rec by replacing each constituent 0-Rec by a corresponding 1-Rec.

Note: a 2-Rec is made of 1-Recs and also made of 0-Recs

Repeat self similar replacement:

A k-Rec is formed from a (k-1)-Rec by replacing each constituent 0-Rec by a corresponding 1-Rec.

Note: 3 ways to think of a k-Rec
- made of (k-1)-Recs
- made of 1-Recs (this will be used in the recursive argument)
- made of 0-Recs (this specifies actual implementation, elementary errors etc & their rates)

Definition: a location is a space-time coordinate in a circuit

(e.g. the gate at the k-th qubit at the j-th time step)

Each location is associated with an operation which can be a state prep, a gate, or a meas. (A resting qubit is associated with the I unitary)

Definition: a fault is a location in which the associated operation deviates from the identity.

e.g. if the ideal gate is $U_{ideal} = e^{i \theta Z}$ but the actual gate is $e^{i (\theta+\delta) Z}$ then the event is given by $U_{ideal}$ * $(\cos \delta \; I + i \sin \delta \; Z)$. The first term is ideal, the second has a fault.

Error -- position information and what happened there
Fault -- positiion and time information, and usually expanded in terms of the Pauli's. We care about the prob/amplitude of faults/sums of faults, but not the detail.

Circuit: consists of locations, each location = (time, space)

level 0 circuit: consists of 0-Rec in each location (including I)

level 1 circuit: replace each 0-Rec in level-0 circuit by corresponding 1-Rec. Can be thought as consisting of 1-Recs, or 0-Recs

level 2 circuit: replace each 0-Rec in level-1 circuit by corresponding 1-Rec's. Can be thought as consisting of 2-Recs, 1-Recs, or 0-Recs.

Repeat this self-similar replacement:

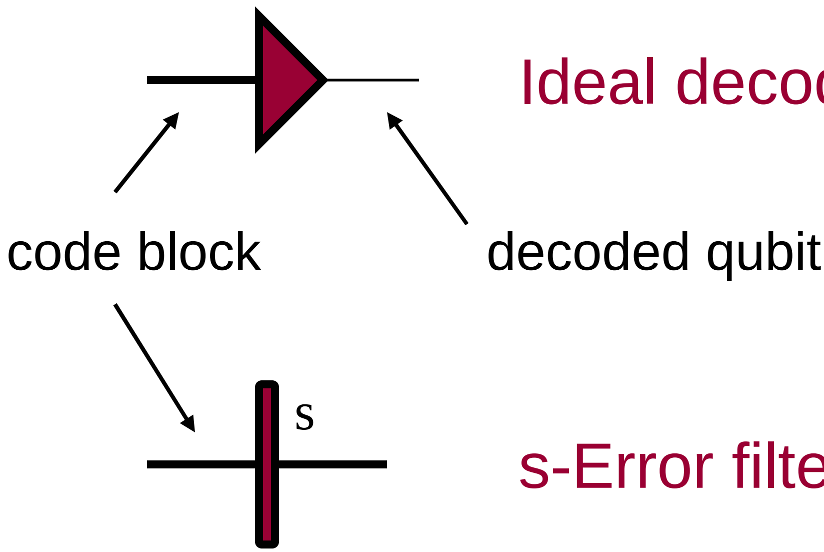
level k circuit: obtained from a level k-1 circuit by replacing 0-Recs with 1-Recs.

- made of k-Recs that defines the original circuit simulated
- made of 1-Recs that are just "plugged in"
- made of 0-Recs that are physical locations

The next several slides contain diagram and words partially recycled from a ppt file by Gottesman.

| |
|---|
| filled -- ideal |
| thick -- encoded |
| thin -- unencoded |

# Ideal decoder and s-filter




Ideal decoder

Corrects errors & decodes state producing an unencoded qubit.

s-Error filter

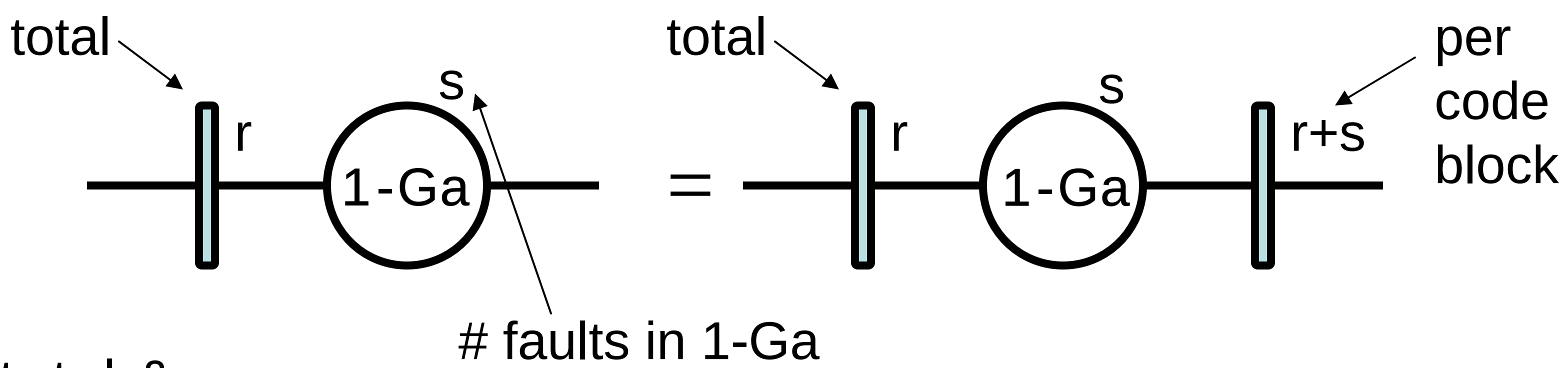
Projects on states that are within s Pauli errors of a valid codeword

These operations cannot be performed using real gates, but useful for defining and proving fault-tolerance.

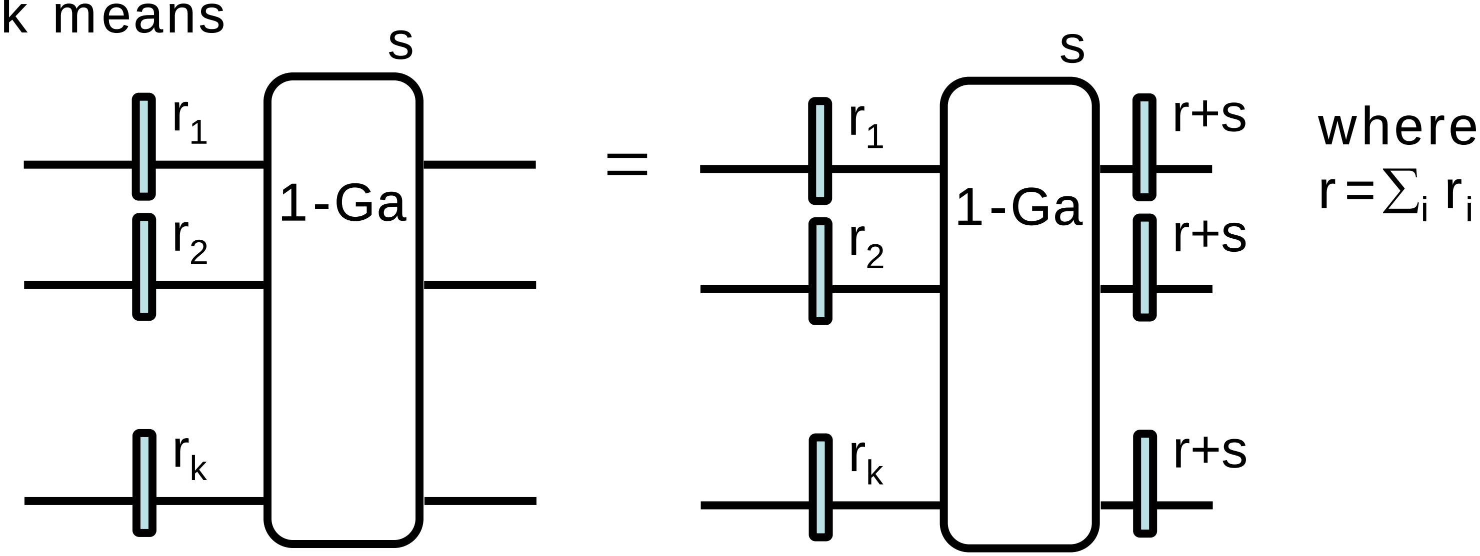
Assume underlying code corrects for t-qubit errors.

# FT gate properties

Ga FT-1: Faults propagate benignly if $r+s \leq t$.

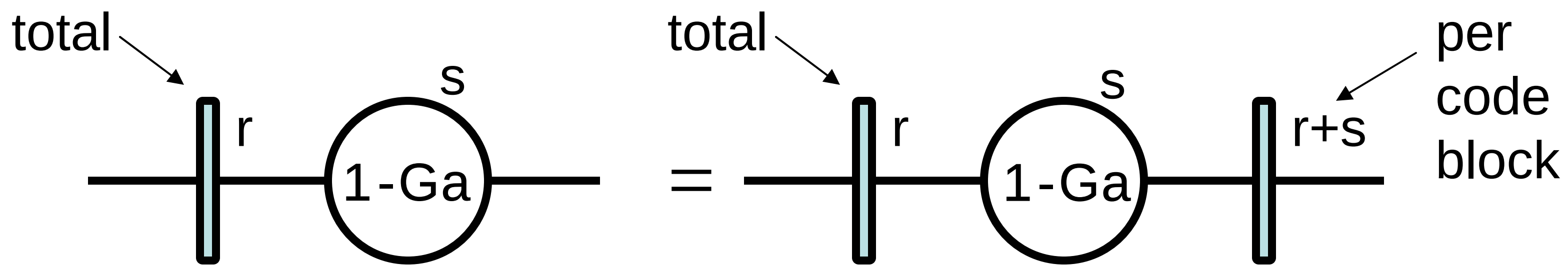



what total &
per block means

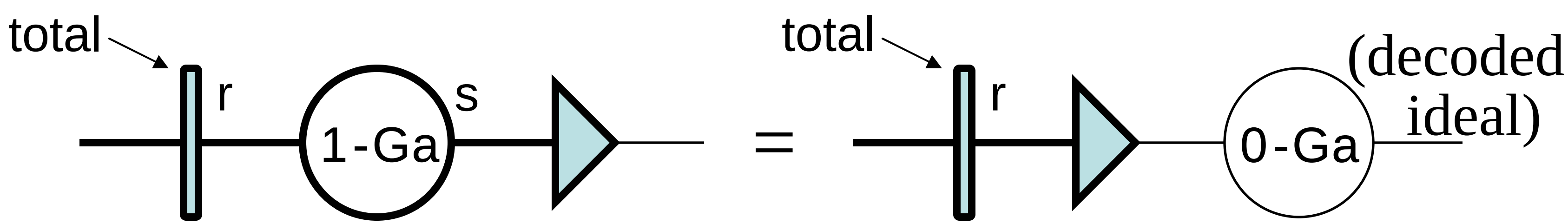


## FT gate properties

Ga FT-1: Faults propagate benignly if $r+s \leq t$

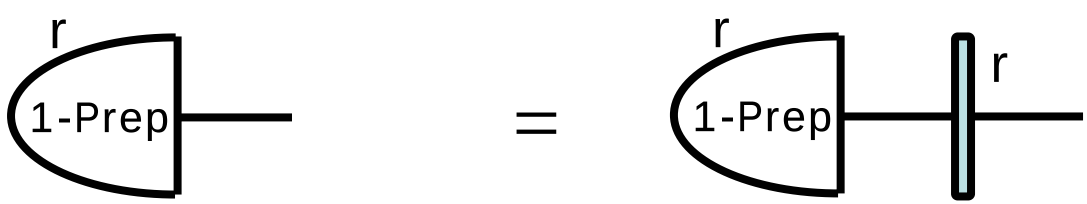



Ga FT-2: performs the encoded gate ideally if $r+s \leq t$

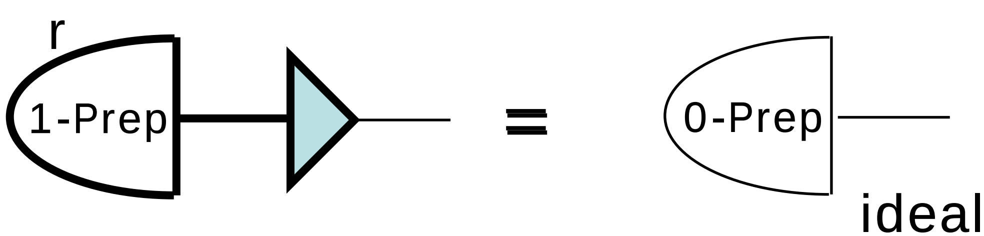


FT meas properties

Prep FT-1: Faults propagate benignly if r $\leq$ t.

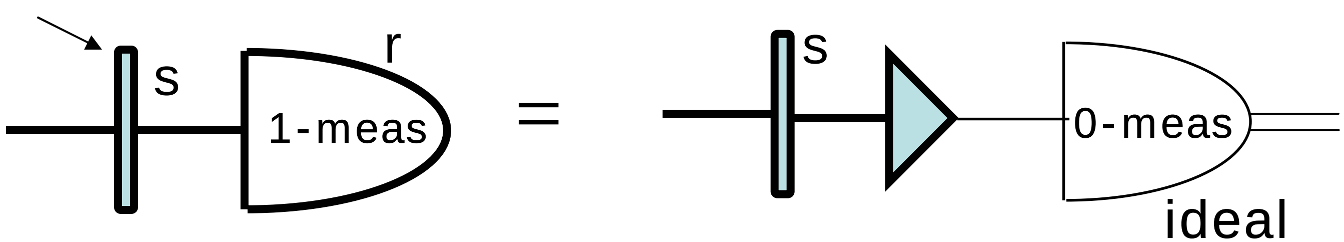



Prep FT-2: prepares the encoded state ideally if r $\leq$ t



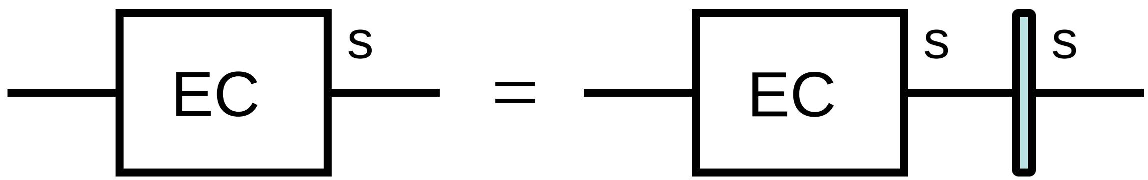
# FT meas properties

Meas FT-2: obtains the ideal outcome if $r+s \leq t$

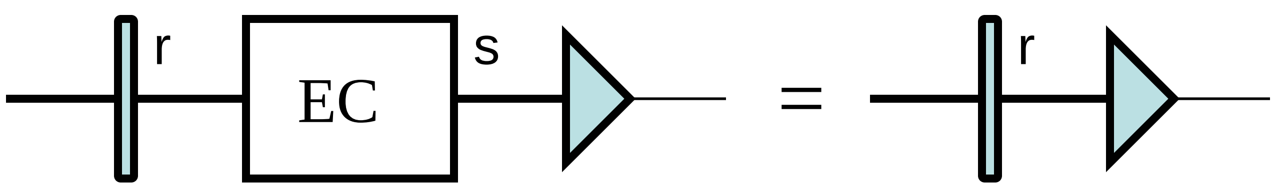


## Error correction properties

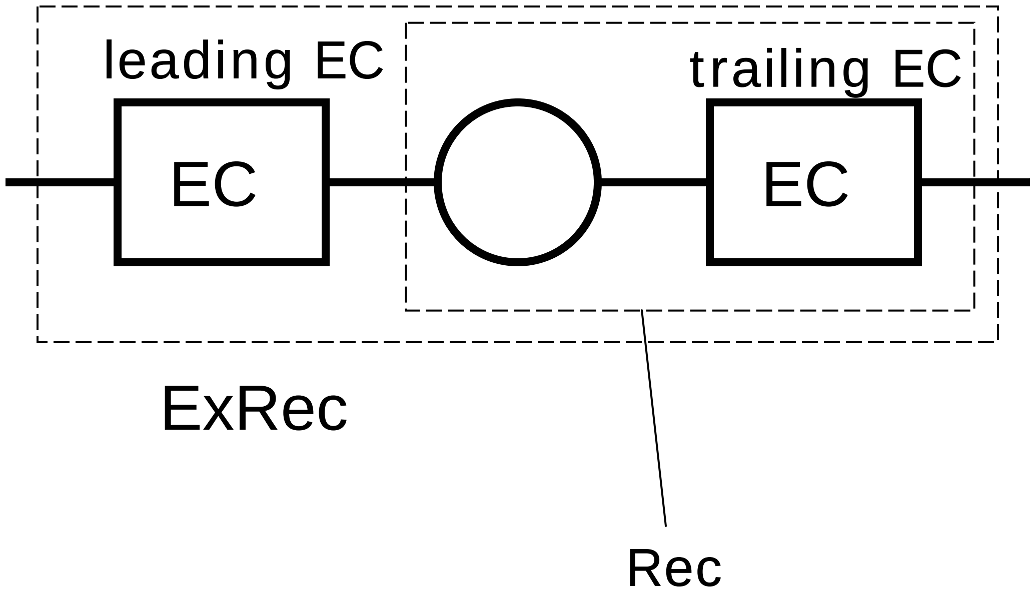
EC FT-1: if s $\leq$ t



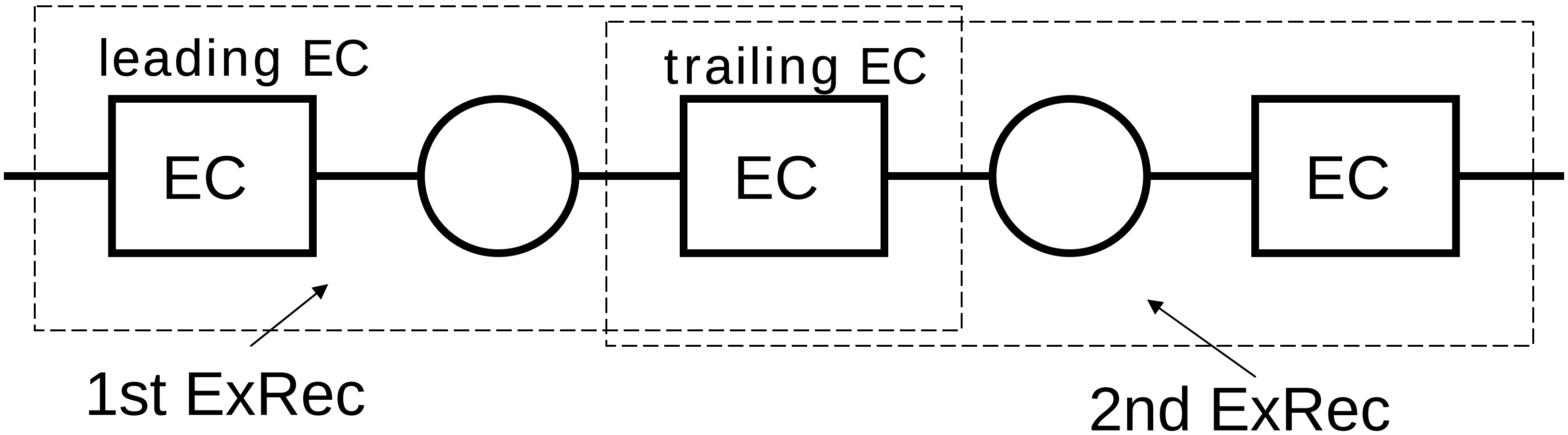

EC FT-2: leaves encoded state alone if r+s $\leq$ t



Def of ExRec: A Rec + EC step before



Def of ExRec: A Rec + EC step before

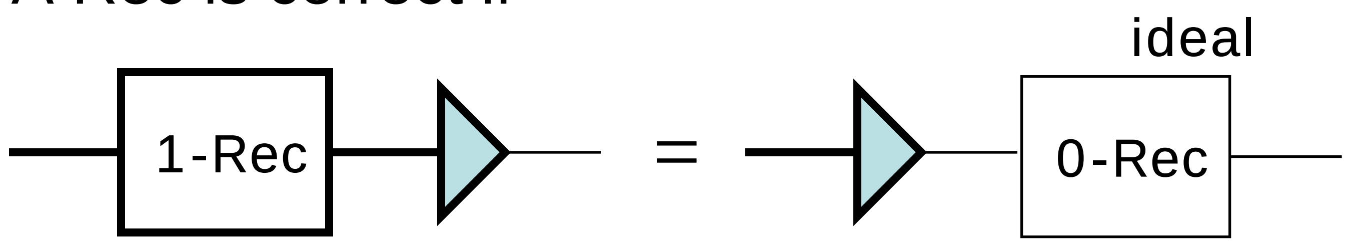



Note: Extended rectangles overlap with each other.

Definition: An ExRec is “good” if it contains $\leq$ t faults

**Definition:** An ExRec is “good” if it contains $\leq$ t faults

**Definition:** A Rec is correct if

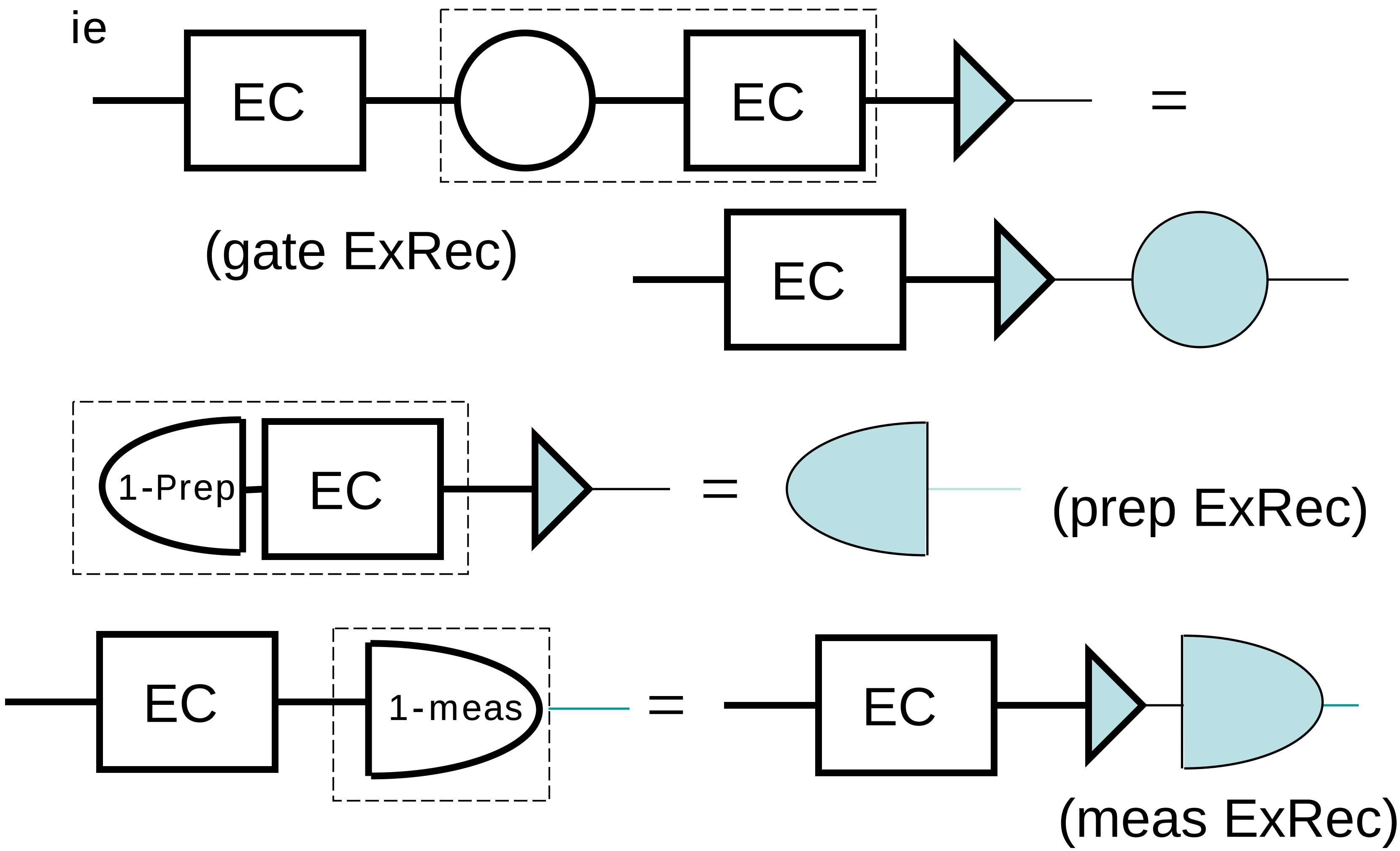



i.e. an ideal decoder can be moved past it to the left

Lemma 1 [Good ⇒ Correct]:

If Ex-Rec good ($\leq$ t faults), then Rec is correct

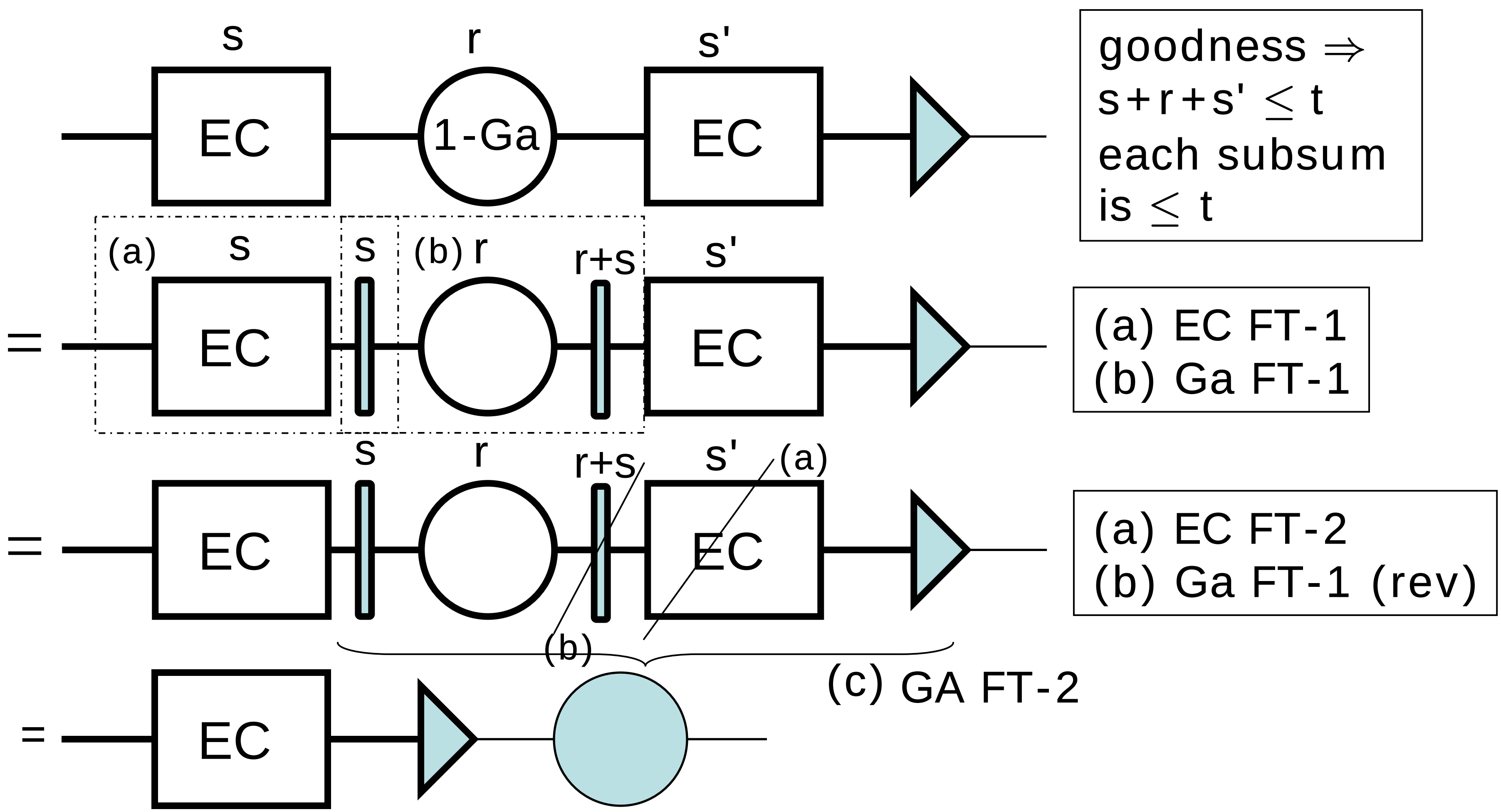
ie



Lemma 1 [Good $\Rightarrow$ Correct]:

If Ex-Rec good ($\leq$ t faults), then Rec is correct

Proof: (gate case only, prep+meas cases: ex)



End of Monday lecture